In the Claims:

1 (currently amended) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including;

a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads,

a relatively low dielectric constant sheath surrounding each wire, and

a mold compound encasing the chip, sheathed wires, and leads having a dielectric constant higher than the dielectric constant of said dielectric sheath.

2 (previously presented) A device as in claim 1 wherein said dielectric sheath comprises a foamed polymer.

3 (previously presented) A device as in claim 1 wherein thickness of the dielectric sheath is 2.5 microns, minimum on each surface.

4 (previously presented) A device as in claim 1 wherein the effective dielectric constant of the sheath surrounding bond wires is in the range of 1.0 to 2.3.

5 (previously presented) A device as in claim 1 wherein the distance between wires is in the range of 50 to 100 microns.

6 (previously presented) A device as in claim 1 wherein the dielectric constant of the molding compound is in the range of 3.8 to 4.2.

7 (previously presented) A device as in claim 1 wherein the mutual capacitance between bond wires is lower by a factor of 3 as compared to a device wherein the medium separating wires has a dielectric constant of 4.0.

8 (previously presented) A device as in claim 1 wherein said dielectric sheath comprises a polyurethane foam.

9 (previously presented) A device as in claim 1 wherein said dielectric sheath comprises a foamed thermoplastic polymer.

10 (previously presented) A device as in claim 1 wherein said device is packaged in a Ball Grid Array package.

11(previously presented) A device as in claim 1 wherein said device is packaged as a leaded surface mount package.

12 (currently amended) A semiconductor device encased within a cavity package having reduced self and mutual capacitance of bond wires, said device including;

a plurality of wire bonds connecting pads on an integrated circuit chip to respective conductive leads of a semiconductor package,

a relatively low dielectric constant sheath surrounding each wire, and

a semiconductor package having leads, a substrate, and a housing shell surrounding an open cavity, said relatively low dielectric constant sheath being disposed within said cavity..

13 (currently amended) A device as in claim 12 wherein said dielectric sheath comprises a foamed polymer.

14 (currently amended) A device as in claim 12 wherein said cavity package shell comprises a ceramic.

15 (currently amended) A device as in claim 12 wherein said dielectric sheath comprises a composite polymer.

16 (previously presented) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including:

a plurality of substantially parallel, closely-spaced wire bonds connecting pads on an integrated circuit chip to conductive leads,

a low dielectric constant sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads..

17 (previously presented and withheld from consideration) A method of packaging a semiconductor device having reduced capacitance bond wires, including the following steps;

attaching a semiconductor chip to a substrate or chip pad of a lead frame,

wire bonding respective ends of a plurality of wires firstly to the pads on the chip, and secondly to leads on said substrate or lead frame,

disposing a polymeric material with foaming agent onto said wire bonds,

allowing the foaming reaction to proceed to near completion,

curing said polymeric material, and

molding a housing or package.

18 (previously presented) A plastic encapsulated semiconductor device having decreased self and mutual bond wire capacitance, said device including:

a plurality of wire bonds connecting pads on an integrated circuit chip to conductive leads.

a foamed polymer sheath surrounding each wire, said sheath covering substantially only said wire and wire connections to said pads on said integrated circuit chip and to said conductive leads, and not covering other portions of said chip and said conductive leads, and

a mold compound encasing the chip, sheathed wires, and leads.